Brazilian Tunable Filter Imager (BTFI)

Detector & Controller

Version 0.1

USP-IAG Universidade de São Paulo

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Original Detector Specifications

- A E2V CCD44-82 2K x 4K full-frame CCD was originally considered

DETECTOR SUB-SYSTEM	
Detector Controller	Commercial CCD camera system. Based on SDSU.
Detector Format	2048^2x4096^2, 2048^2 pixels focal plane area each with 20482 blanked 20482 frame transfer area, possible L3CCD
Detector Pixels	13.5 microns (could also be 15 micron pixels)
Number detectors	Two Cameras, therefore 2 x 2048^2x4096^2 CCDs
Detector Channels	Diffracted channel to have best CCD detector. Zero-order straight-through CCD detector will operate excess photons and will be used only to acquire, guide and monitor PSF.

The E2V CCD 44-82

TYPICAL PERFORMANCE (at 173 K)

Pixel readout frequency	20 - 1000	kHz
Output amplifier sensitivity	6.0	µV/e⁻
Peak signal	200	ke⁻/pixel
Spectral range	200 - 1060	nm
Readout noise (at 20 kHz)	2.5	e⁻ rms
QE at 500 nm	90	%
Charge transfer efficiency	99.9995	%

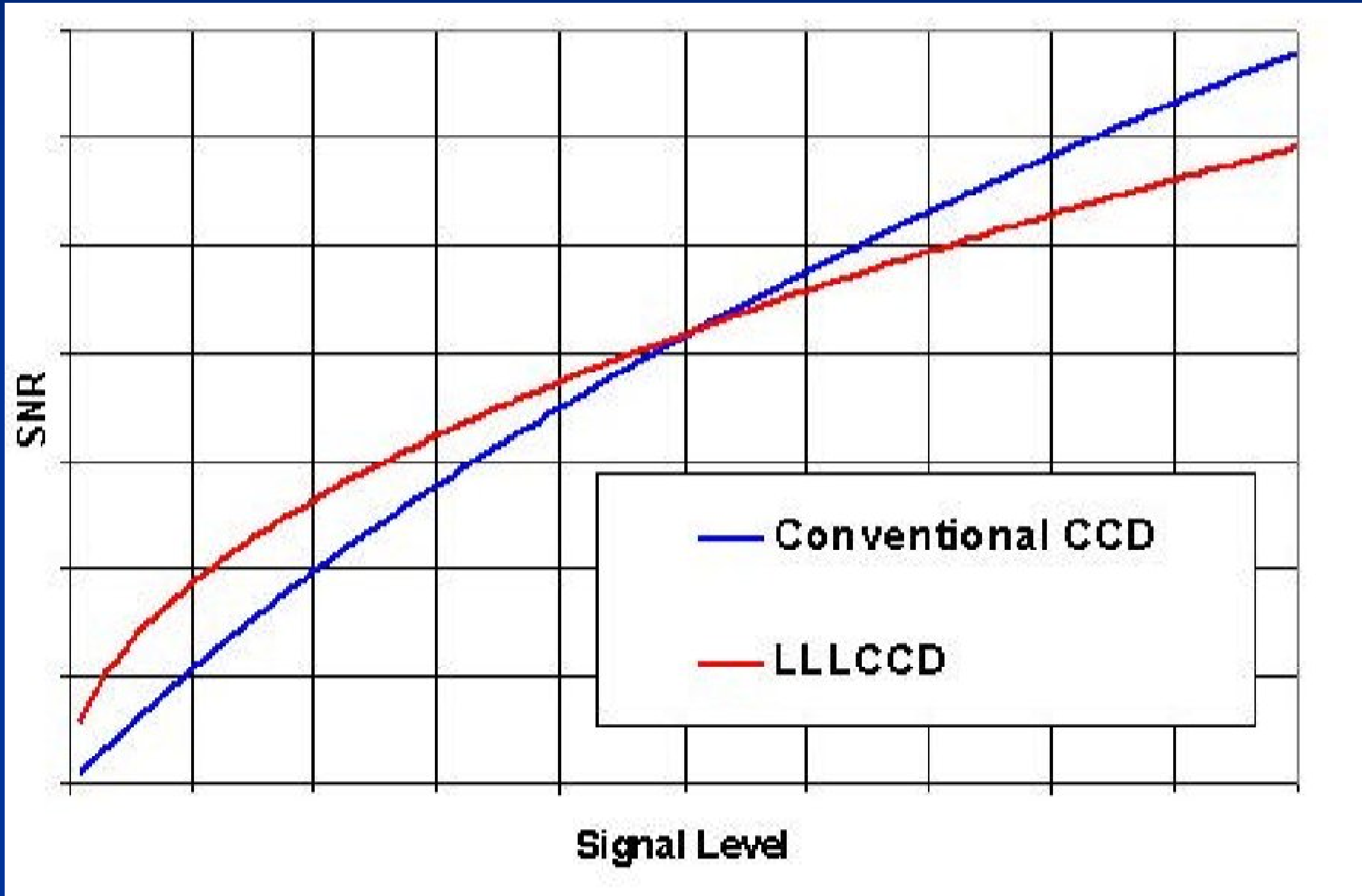
GENERAL DATA

Format

Image area	30.7 x 61.4	mm
Active pixels (H)	2048	
(V)	4096 + 6	
Pixel size	15 x 15	µm
Number of output amplifiers	2	
Number of underscan (serial) pixels	50	

The device has a 100% fill factor.

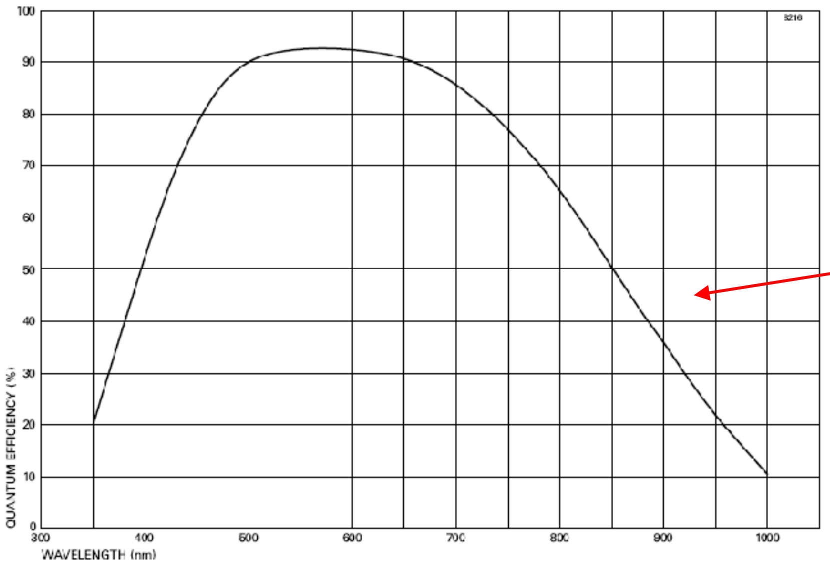
The L3CCD Advantage



L3CCD - General Description

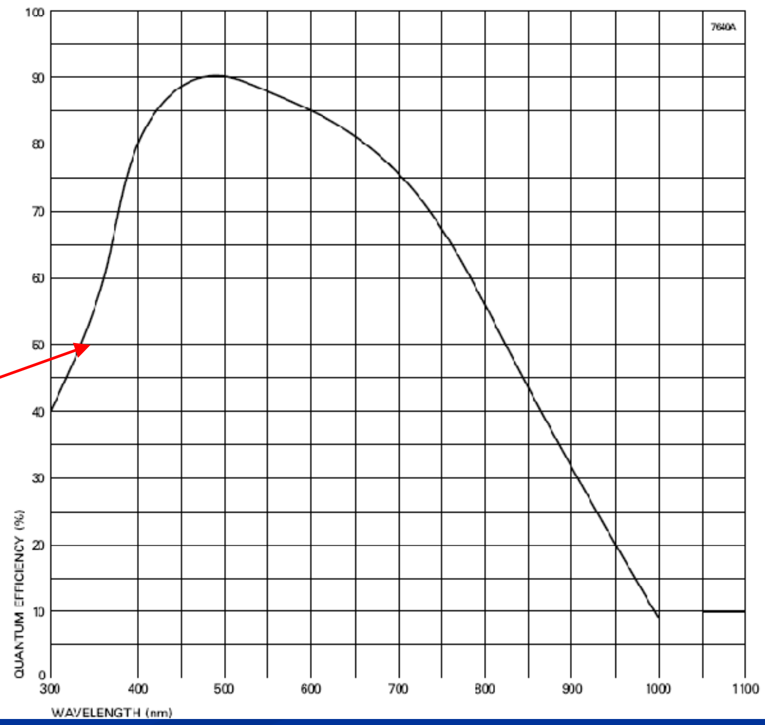
- Conventional CCD + longer serial register
- Serial register with 1 high voltage (HV) clock
- Electron multiplication (EM) is produced due to the avalanche effect, driven by the HV clock
- Gain per pixel R~1%, total gain G~10000 $G = (1 + R)^n$
- EM gain is adjusted by HV level
- Capable of running quieter and faster:
  - Classic CCD44-82: 2.5e- @ 100KHz; 8e- @ 2MHz
  - EM CCD201: <1e- @ 15 MHz

Figure 3: TYPICAL SPECTRAL RESPONSE (At −20 °C, no window, midband coating)



L3CCD

TYPICAL SPECTRAL RESPONSE
(At −90 °C, measured with astronomy broadband AR coating)



CCD44-82

The L3CCD

CCD201 available from E2V now (frame transfer)

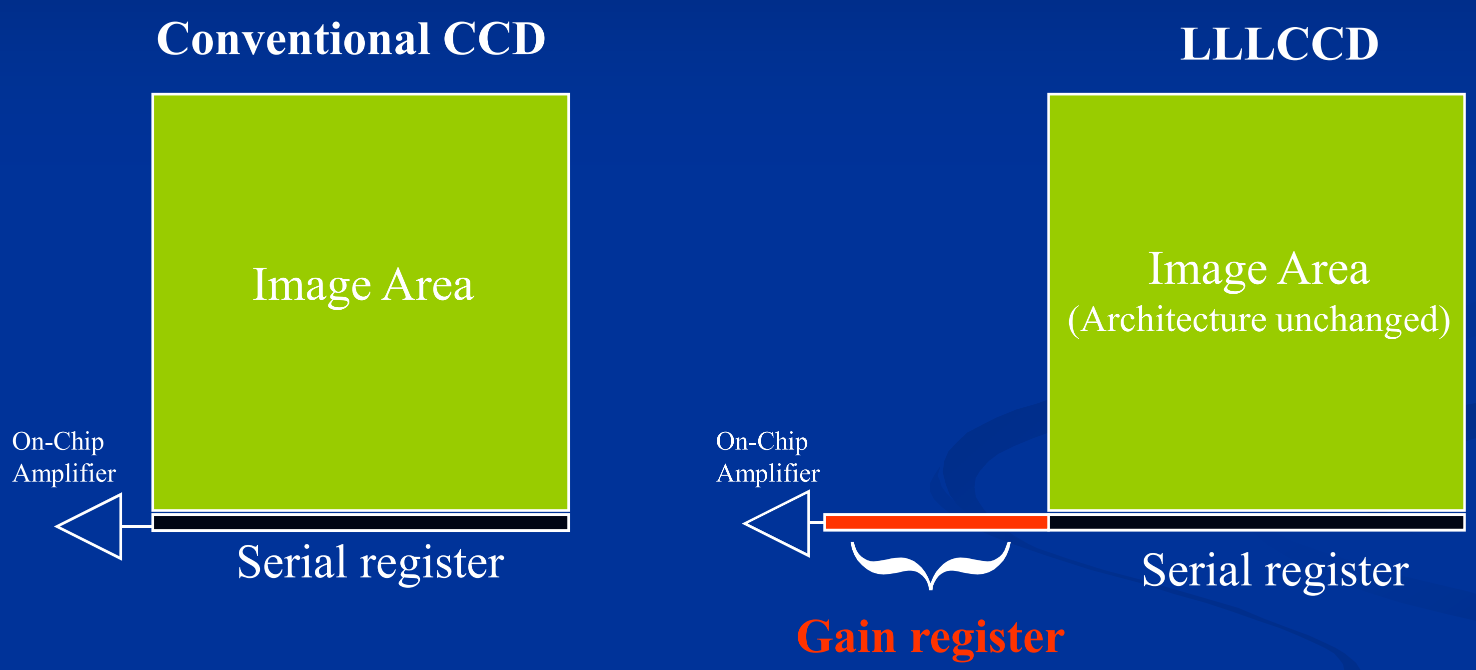
GENERAL DATA

Active image area	13.3 x 13.3 mm
Image section active pixels	1024 (H) x 1024 (V)
Image pixel size	13 x 13 µm
Number of output amplifiers	2
Fill factor	100%
Additional dark reference columns	32
Additional overscan rows	8

E2V: CCD207-40 1600*1600 full-frame L3CCD with 16 um pixels will be available in 2008 – Received preliminary datasheet

L3CCD

the gain register

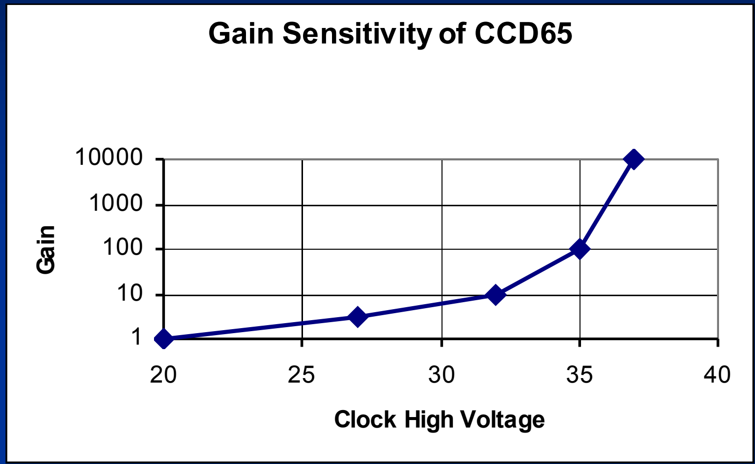


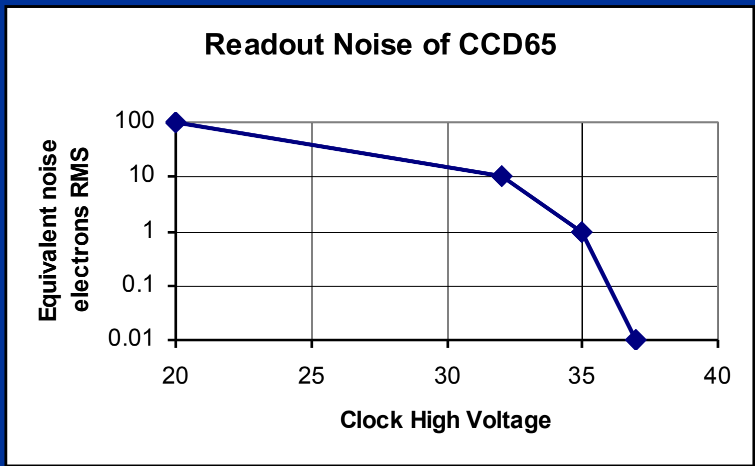
The Gain Register can be added to any existing design

L3CCD – Theory of Operation

- Gain electrode energized. Charge packets accelerated strongly into deep potential well.
- Energetic electrons loose energy through creation of more charge carriers (analogous to multiplication effects in the dynodes of a photo-multiplier) .
- Clocking continues but each time the charge packets pass through the gain electrode, further amplification is produced. Gain per stage is low, <1.015, however the number of stages is high so the total gain can easily exceed 10,00
- Readout noise is decoupled from readout speed

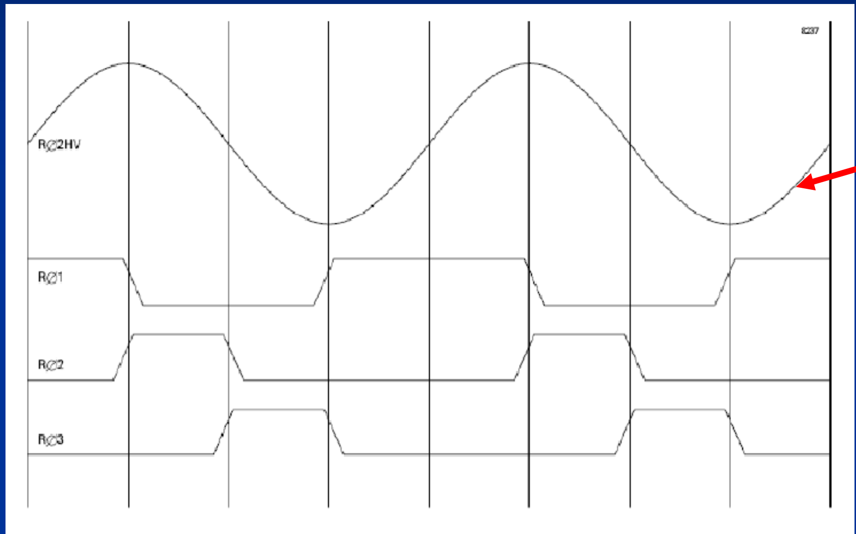
L3CCD – Clock Voltage & Gain



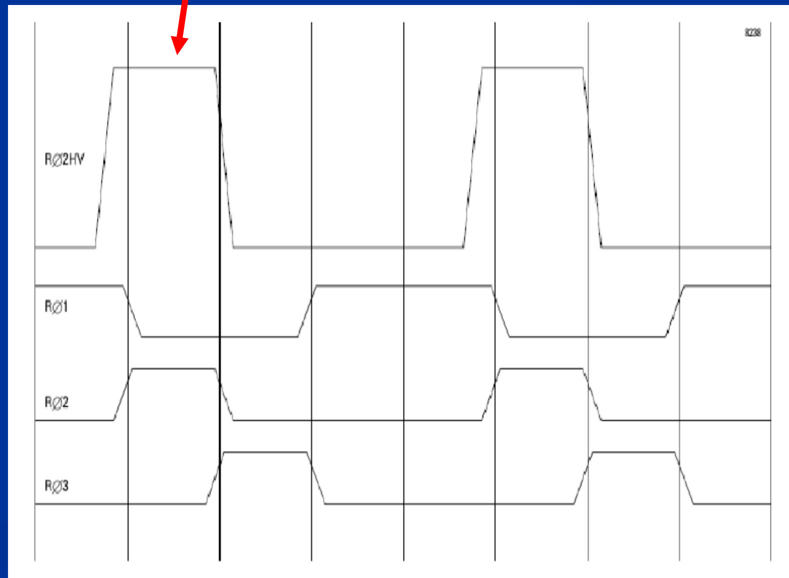


The Multiplication Register has a gain strongly dependant on the clock voltage

L3CCD - Clock Waveforms



High voltage waveform can be trapezoidal or sinusoidal, each of them with pros/cons



L3CCD - Noise Sources

- CIC
  - a.k.a. "spurious charge"; produced in image area
  - Most significant noise source in EMCCDs, not in CCDs
  - Reduced when using "non-inverted mode"
  - 0.005 (E2V) < CIC < 0.02 (WHT) expected for our detector
- Multiplication noise
  - Produced in multiplication register
  - Seen in a photon transfer curve as variance = 2 x mean
  - Implication in noise: $\sigma_{EMCCD} = \sigma_{CCD} \times \sqrt{2}$, or half QE
- Dark current depends on mode of operation
  - Low when exposing, e.g. using "inverted mode"
  - High when reading out, e.g. in non-inverted mode

L3CCD and Photon Couting

- In Photon Counting mode the pixel values are thresholded and represent one photon-electron a pre-determined value is exceeded. Readout rates can be as hight as 35MHz. This mode will only work at low illumination levels (around 0.1 counts per frame per pixel) or loss of QE and linearity will occur due to coincidence.

CCDs and SNR

Conventional CCD SNR Equation

$$SNR = Q.I.t.\left[Q.t.(I + B_{SKY}) + N_r^2\right]^{-0.5}$$

Q = Quantum Efficiency
I = Photons per pixel per second
t = Integration time in seconds
B_{SKY} = Sky background in photons per pixel per second
N_r = Amplifier (read-out) noise in electrons RMS

Very hard to get **Nr** < 3e, and then only by slowing down the readout significantly. At TV frame rates, noise > 50e

LLLCCD SNR Equation

$$SNR = Q.I.t.F_n.\left[Q.t.F_n.(I + B_{SKY}) + (N_r/G)^2\right]^{-0.5}$$

G = Gain of the Gain Register
F_n = Multiplication Noise factor = 0.5

With G set sufficiently high, this term goes to zero, even at TV frame rates.

Unfortunately, the problem of multiplication noise is introduced

In Photon Counting Mode: $SNR = Q.I.t.[Q.t.(I + B_{SKY})]^{-0.5}$

L3CCD – Operational Regimes

1) Unity Gain Mode.

The CCD operates normally with the SNR dictated by the photon shot noise added in quadrature with the amplifier read noise. In general a slow readout is required (300KPix/second) to obtain low read noise (4 electrons would be typical). Higher readout speeds possible but there will be a trade-off with the read-noise.

2) High Gain Mode.

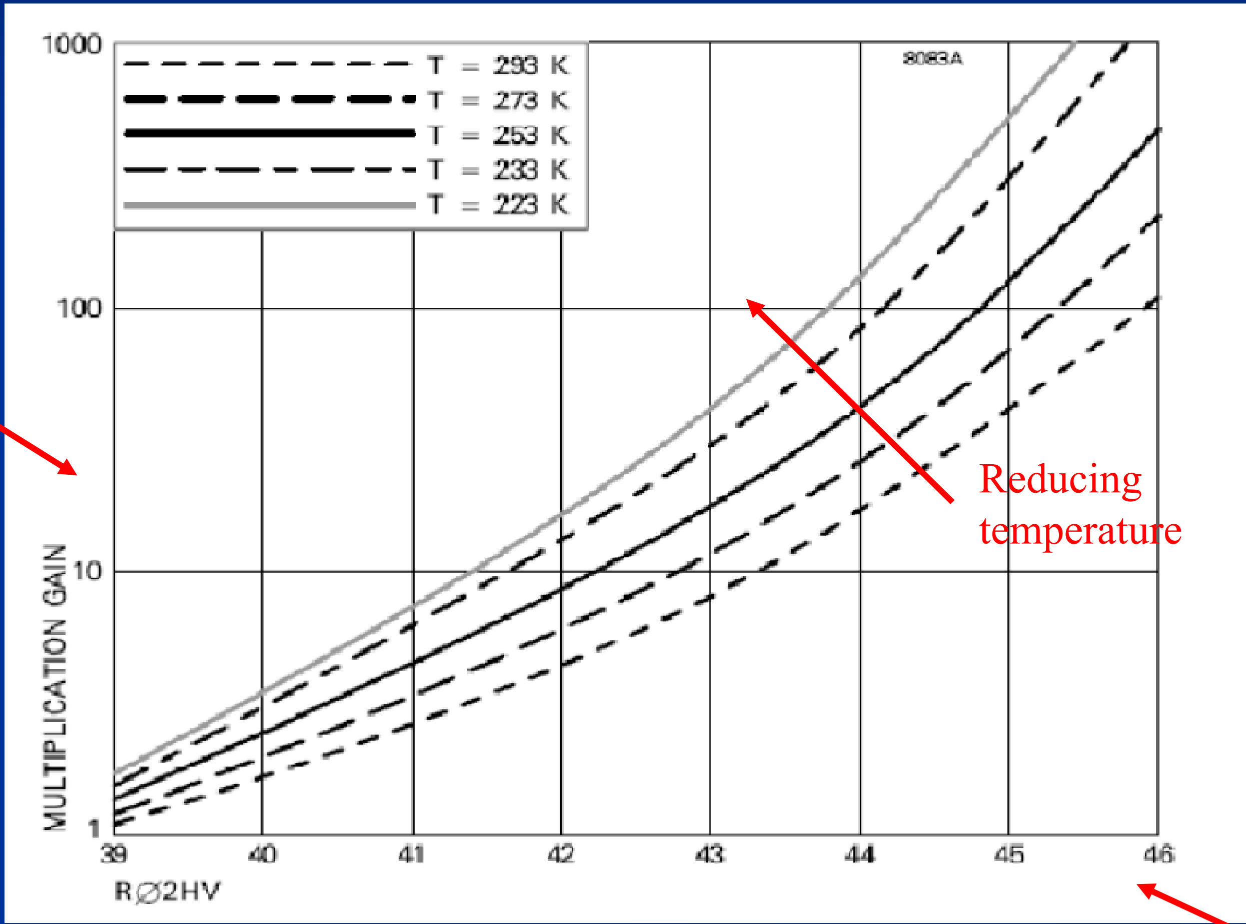
Gain set sufficiently high to make noise in the readout amplifier of the CCD negligible. The drawback is the introduction of Multiplication Noise that reduces the SNR by a factor of 1.4. Read noise is de-coupled from read-out speed. Very high speed readout possible, up to 11MPixels per second, although in practice the frame rate will probably be limited by factors external to the CCD.

3) Photon Counting Mode.

Gain is again set high but the video waveform is passed through a comparator. Each trigger of the comparator is then treated as a single photo-electron of equal weight. Multiplication noise is thus eliminated. Risk of coincidence losses at higher illumination levels.

EMCCD - Peculiarities

Multiplication Gain (log scale)



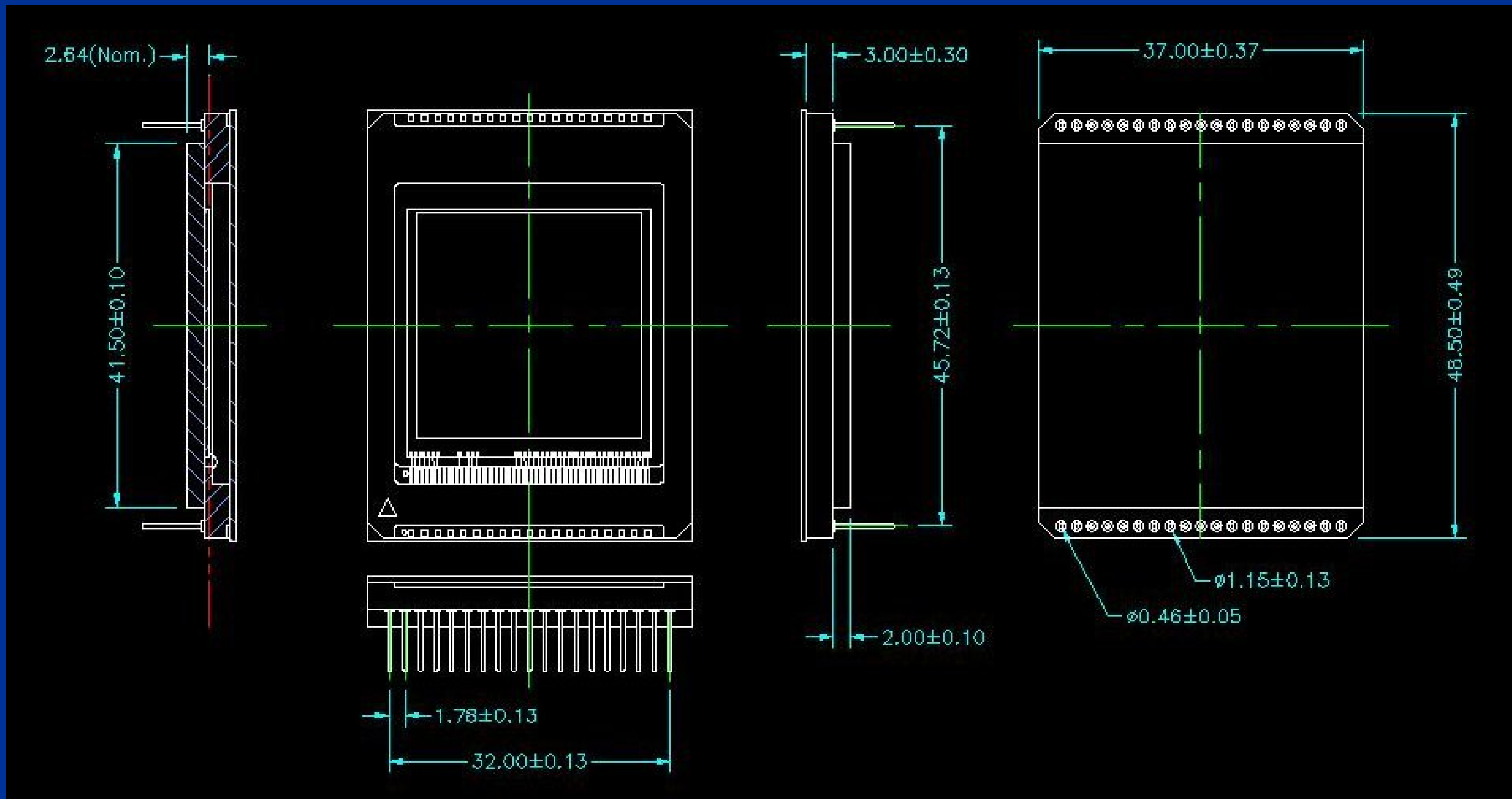
Reducing temperature

High voltage level

High voltage and temperature stability are important for constant multiplication gain

EMCCD package

- Ceramic package makes accurate temperature control difficult



EMCCD - Beware of

- There will be a compromise when dealing with CIC and dark current, regarding temperature, inverted mode
- It seems conservative to use other groups' numbers for now, but it is required to go through a detailed detector characterization phase in order to understand detector limitations that will affect instrument performance
- We need good control of:
  - Temperature (<1ºC)
  - High voltage clock stability (<1%)

Key Areas for Controller Selection

- Goal for now: identify detector areas that are key in deciding controller specs
- 2 controller available:
  - SDSU + HV clock board
  - Daigle's controller
- HV clock waveform options: sine or trapezoidal
  - Trapezoidal (SDSU) is better for linearity in conventional mode
  - Sine (Daigle's) is better for reducing thermal effects, important when in high gain mode
- Readout speed requirements for photon counting
  - Limited readout speed (SDSU) can be sufficient for low fluxes
  - Daigle's can achieve much faster readout than SDSU

SDSU Controller for L3CCD

- Most SOAR instruments use SDSU-2 controllers. We have the option of using a similar controller for maintenance purposes. SDSU-3 with the new Motorola DSP 56303 is similar to SDSU-2 but faster (12,5Mpixel/s). Given L3CCD only has one output amplifier, we will be limited by ADC sampling frequency (~2 MHz @ 16bits)
- The high voltage multiplication clock needs to be added, but ATC is willing to supply such board